

1. Features

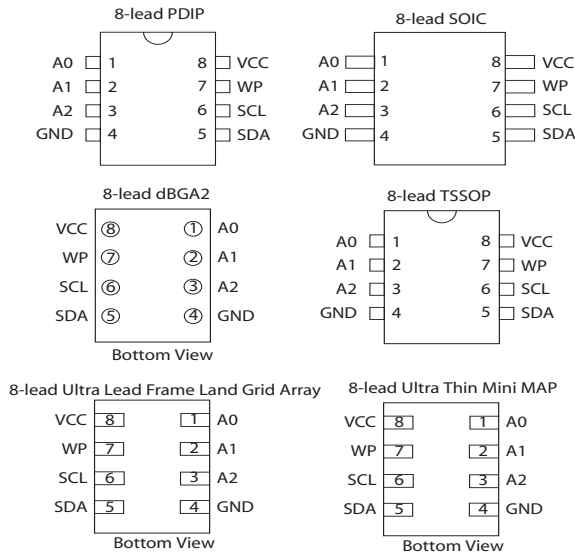
- Low-voltage and Standard-voltage Operation
 - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized as 16,384 x 8
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (5.5V, 2.5V), and 400 kHz (1.8V) Compatibility
- Write Protect Pin for Hardware and Software Data Protection
- 64-byte Page Write Mode (Partial Page Writes Allowed)
- Self-timed Write Cycle (5 ms Max)
- High Reliability
 - Endurance: One Million Write Cycles
 - Data Retention: 40 Years
- Lead-free/Halogen-free
- 8-lead JEDEC PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Thin Mini MAP, 8-lead Ultra Lead Frame Land Grid Array (ULA), 8-lead TSSOP, and 8-ball dBGGA2 Packages
- Die Sales: Wafer Form, Tape and Reel and Bumped Wafers

2. Description

The AT24C128B provides 131,072 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 16,384 words of 8 bits each. The device's cascadable feature allows up to eight devices to share a common two-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space-saving 8-lead JEDEC PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Thin Mini MAP, 8-lead Ultra Lead Frame Land Grid Array (ULA), 8-lead TSSOP, and 8-ball dBGGA2 packages. In addition, the entire family is available in a 1.8V (5.5V to 3.6V) version.

Table 0-1. Pin Configurations

Pin Name	Function
A0–A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground



Two-wire Serial EEPROM

128K (16,384 x 8)

AT24C128B

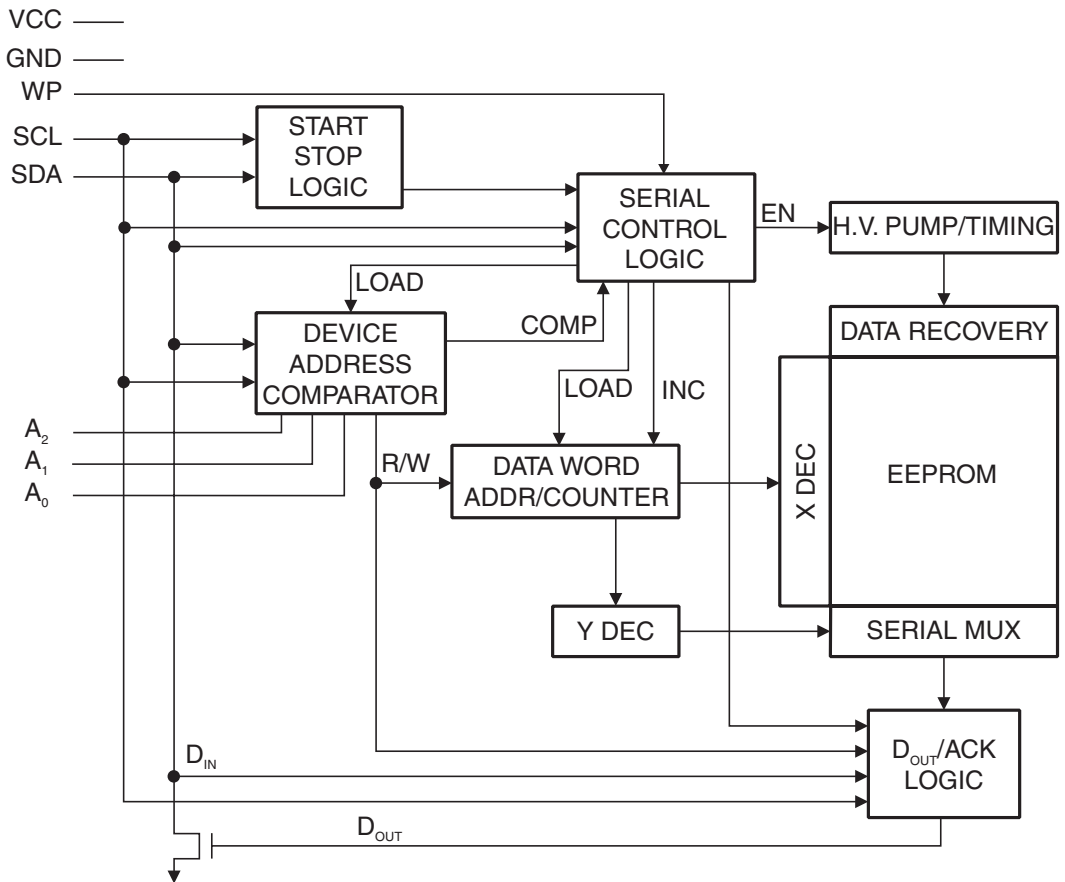


3. Absolute Maximum Ratings*

Operating Temperature.....	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current.....	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 3-1. Block Diagram





5. Memory Organization

AT24C128B, 128K SERIAL EEPROM: The 128K is internally organized as 256 pages of 64 bytes each. Random word addressing requires a 14-bit data word address.

Table 5-1. Pin Capacitance⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = +1.8\text{V}$ to 5.5V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0\text{V}$
C_{IN}	Input Capacitance (A_0 , A_1 , SCL)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

Table 5-2. DC Characteristics

Applicable over recommended operating range from: $T_{AI} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$ (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
I_{CC1}	Supply Current	$V_{CC} = 5.0\text{V}$	READ at 400 kHz		1.0	2.0	mA
I_{CC2}	Supply Current	$V_{CC} = 5.0\text{V}$	WRITE at 400 kHz		2.0	3.0	mA
I_{SB1}	Standby Current (1.8V option)	$V_{CC} = 1.8\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}			1.0	μA
		$V_{CC} = 5.5\text{V}$				6.0	μA
I_{LI}	Input Leakage Current $V_{CC} = 5.0\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}			0.10	3.0	μA
I_{LO}	Output Leakage Current $V_{CC} = 5.0\text{V}$	$V_{OUT} = V_{CC}$ or V_{SS}			0.05	3.0	μA
V_{IL}	Input Low Level ⁽¹⁾			-0.6		$V_{CC} \times 0.3$	V
V_{IH}	Input High Level ⁽¹⁾			$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL2}	Output Low Level	$V_{CC} = 3.0\text{V}$	$I_{OL} = 2.1\text{ mA}$			0.4	V
V_{OL1}	Output Low Level	$V_{CC} = 1.8\text{V}$	$I_{OL} = 0.15\text{ mA}$			0.2	V

Notes: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 5-3. AC Characteristics (Industrial Temperature)

Applicable over recommended operating range from $T_{AI} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $CL = 100\text{ pF}$ (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.8-volt		2.5, 5.5-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3		0.4		μs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		μs
t_i	Noise Suppression Time ⁽¹⁾		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.05	0.9	0.05	0.55	μs
t_{BUF}	Time the bus must be free before a new transmission can start ⁽¹⁾	1.3		0.5		μs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		μs
$t_{SU.STA}$	Start Set-up Time	0.6		0.25		μs
$t_{HD.DAT}$	Data In Hold Time	0		0		μs
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_R	Inputs Rise Time ⁽¹⁾		0.3		0.3	μs
t_F	Inputs Fall Time ⁽¹⁾		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		0.25		μs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance ⁽¹⁾	25°C, Page Mode, 3.3V	1,000,000				Write Cycles

Notes: 1. This parameter is ensured by characterization and is not 100% tested.

2. AC measurement conditions:

R_L (connects to V_{CC}): 1.3 k Ω (2.5V, 5.5V), 10 k Ω (1.8V)

Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}

Input rise and fall times: $\leq 50\text{ ns}$

Input and output timing reference voltages: 0.5 V_{CC}



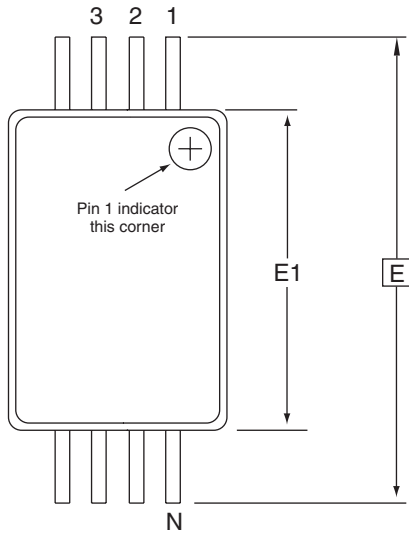
10. AT24C128B Ordering Information

Ordering Code	Voltage	Package	Operation Range
AT24C128B-PU (Bulk Form Only)	1.8	8P3	Lead-free/Halogen-free Industrial Temperature (-40°C to 85°C)
AT24C128BN-SH-B ⁽¹⁾ (NiPdAu Lead Finish)	1.8	8S1	
AT24C128BN-SH-T ⁽²⁾ (NiPdAu Lead Finish)	1.8	8S1	
AT24C128B-TH-B ⁽¹⁾ (NiPdAu Lead Finish)	1.8	8A2	
AT24C128B-TH-T ⁽²⁾ (NiPdAu Lead Finish)	1.8	8A2	
AT24C128BY6-YH-T ⁽²⁾ (NiPdAu Lead Finish)	1.8	8Y6	
AT24C128BD3-DH-T ⁽²⁾ (NiPdAu Lead Finish)	1.8	8D3	
AT24C128BU2-UU-T ⁽²⁾	1.8	8U2-1	Industrial Temperature (-40°C to 85°C)
AT24C128B-W-11 ⁽³⁾	1.8	Die Sale	

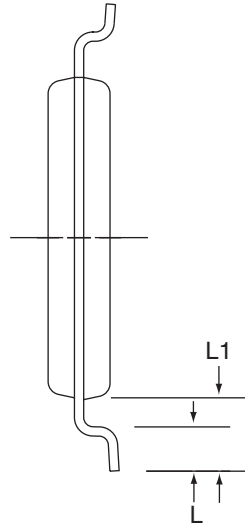
- Notes:
1. "-B" denotes bulk.
 2. "-T" denotes and tape and reel. SOIC = 4K. TSSOP, dBGA2, and Mini MAP = 5k. SAP = 3K.
 3. Available in tape and reel and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Interface Marketing.

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.00 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Mini MAP, Dual No Lead Package, (DFN), (MLP2x3mm)
8D3	8-lead, 1.80 mm x 2.20 mm Body, Ultra Lead Frame Land Grid Array (ULA)
8U2-1	8-ball, die Ball Grid Array Package (dBGA2)
Options	
-1.8	Low-voltage (1.8V to 5.5V)

8A2 - TSSOP



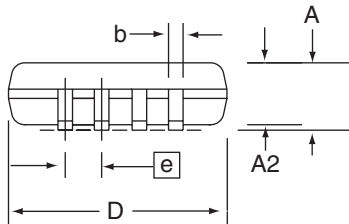
Top View



End View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E	6.40 BSC			
E1	4.30	4.40	4.50	3, 5
A	-	-	1.20	
A2	0.80	1.00	1.05	
b	0.19	-	0.30	4
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	1.00 REF			



Side View

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
 2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
 3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
 4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
 5. Dimension D and E1 to be determined at Datum Plane H.



2325 Orchard Parkway
San Jose, CA 95131

TITLE

8A2, 8-lead, 4.4 mm Body, Plastic
Thin Shrink Small Outline Package (TSSOP)

DRAWING NO.

8A2

REV.

B